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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,924	05/30/2001	Nobuaki Hashimoto	109681	6373

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EXAMINER

TRAN, TAN N

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/856,924

Applicant(s)

HASHIMOTO ET AL.

Examiner

TAN N TRAN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on amendment filed on 07/03/03.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 and 33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 7-9 and 13-15 is/are allowed.
- 6) ☒ Claim(s) 1-6, 10-12, 16-19, 33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(c)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,4,5,10,17,33 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (2002/0003308) of record.

With regard to claim 1, Kim et al. discloses a substrate 20 including a plurality of holes 22 and a surface over which an interconnecting pattern 23 is formed, part of the interconnecting pattern 23 being superposed over the holes 22; the interconnecting pattern not formed on inner surface of the holes 22; a semiconductor chip 31 disposed over another surface of the substrate 20 and including a plurality of bonding pads serves as electrodes to be positioned over the holes 22; and conductive posts 33 provided contiguously on the bonding pads and within the holes 22 to be electrically connected to the interconnecting pattern 23. (Note lines 1-8, page 2, fig. 9 of Kim et al.).

With regard to claim 4, Kim et al. discloses part of the interconnecting pattern 23 closes the holes 22. (Note fig. 9 of Kim et al.).

With regard to claim 5, Kim et al. discloses the interconnecting pattern 23 includes a plurality of interconnecting lines; and wherein two or more interconnecting lines extend over each of the holes 22. (Note fig. 9 of Kim et al.).

With regard to claim 10, Kim et al. discloses the conductive posts 33 are a plurality of layered bumps. (Note fig. 9 of Kim et al.).

With regard to claim 17, Kim et al. discloses the semiconductor chip 31 is mounted face-down to the substrate 20. (Note fig. 9 of Kim et al.).

With regard to claim 33, Kim et al. discloses there is a space between a conductive post 33 and an inner surface of each of the holes 22. (Note fig. 9 of Kim et al.).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2,6,18,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (2002/0003308).

With regard to claim 2, Kim et al. discloses an encapsulating body 40 for encapsulating the semiconductor chip 31 and substrate 20. (Note fig. 9 of Kim et al.). Kim et al. disclose all the claimed subject matter except for encapsulating material is resin. However, it would have been obvious to one of ordinary skill in the art to form encapsulating material is resin in order to secure to bond the semiconductor chip 31 and semiconductor substrate 20.

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With regard to claim 6, Kim et al. discloses all claimed invention as in claim 1, except the other surface of the substrate 20 is roughed. However, it would have been obvious to one of ordinary skill in the art to form Kim et al.'s case having surface of the substrate is roughed because such element is conventional in the art in order to make the encapsulating body is more stable.

With regard to claims 18 and 19, Kim et al. discloses all claimed invention as in claim 1, except a circuit board and electronic instrument provided with the semiconductor device. However, it would have been obvious to one of ordinary skill in the art to form Kim et al.'s case on a circuit board or an electronic instrument provided with the semiconductor device because such structure is conventional in the art for forming the semiconductor integrated circuit package.

Claims 3,11,12,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (2002/0003308) Otsuka (US 5,949,142) of record.

With regard to claim 3, Kim et al. does not disclose the resin is an anisotropic conductive material containing conductive particles and the conductive posts are electrically connected to interconnecting pattern through the conductive particles.

However, Otsuka discloses the resin is an anisotropic conductive material 6 containing conductive particles 6a and the conductive posts (4c,4d) are electrically connected to interconnecting pattern 4b through the conductive particles 6a. (Note lines 13-17, column 4, figs 1, 3 of Otsuka).

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Therefore, it would have been obvious to one of ordinary skill in the art to form the Kim et al.'s device having the resin is an anisotropic conductive material containing conductive particles and the conductive posts are electrically connected to interconnecting pattern through the conductive particles such as taught by Otsuka in order to have electrically connection between the semiconductor chip and conductive pattern.

With regard to claim 11, Kim et al. discloses the bump 33 formed on the electrode pad. (Note lines 1-8, page 2, fig. 9 of Kim et al.). Kim et al. does not disclose second bumps formed on the first bumps.

However, Otsuka discloses the bumps (4a, 4c) include first bumps 4a formed on the electrodes and second bumps 4c formed on the first bumps 4a. (Note figs 1, 3 of Otsuka).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Kim et al.'s device having second bumps formed on the first bumps such as taught by Otsuka in order to increase electrically connection conductivity between the chip and connecting pattern.

With regard to claim 12, Otsuka and Kim et al. disclose all claimed invention as in claims 1 and 10, except at least the first bumps are ball bumps. However, it would have been obvious to one of ordinary skill in the art to form Otsuka and Kim et al.'s case having at least the first bumps are ball bumps in order to form the conductive particles in a thermosetting resin for electrically connecting to the semiconductor chip via an insulating layer more easy.

With regard to claim 16, Otsuka and Kim et al. disclose all claimed invention as in claims 1 and 11, except the first bumps and the second bumps are formed of the same material. However, it would have been obvious to one of ordinary skill in the art to form Otsuka and Kim

et al.'s case having the first bumps and the second bumps are formed of the same material in order to simplify the processing steps.

Allowable Subject Matter

3. Claims 7-9, 13-15 are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as a recognition hole is formed in the substrate at position differing from the holes; and wherein a recognition pattern is formed over the recognition hole on the side of a surface of the substrate including the interconnecting pattern in claim 7, and the second bumps are formed of a metal which has a melting point lower than the melting point of the first bumps in claim 13.

Response to Arguments

4. Applicant's arguments filed 07/03/03 have been fully considered but they are not persuasive.

It is argued, at pages 6,7 of the remarks, that "Otsuka does not disclose the interconnecting pattern not formed on intersurfaces of the holes" and "Both Otsuka and Grupen-Shemansky do not disclose an interconnecting pattern not form on intersurfaces of the holes". However, fig. 9 of Kim et al. does show part of the interconnecting pattern 23 being superposed over the holes 22.

It is argued, at page 6 of the remark, that "Otsuka does not disclose conductive posts provided contiguously on the electrode". However, lines 1-8, page 2, fig. 9 of Kim et al. does

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show conductive posts 33 provided contiguously on the bonding pads and within the holes 22 to be electrically connected to the interconnecting pattern 23. Since claim 1 does not recited conductive posts provided contiguously on the electrode and within the hole, applicant's claim 1 does not distinguish over the Kim et al. reference.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the

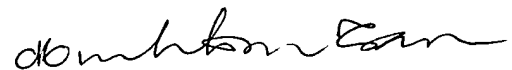
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organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

August 2003



Minhloan Tran
Primary Examiner
Art Unit 2826